

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A modulator comprising:

a PLL circuit which detects a phase difference between an input signal and a reference signal, wherein the PLL circuit outputs a signal of which an undesired frequency component is removed;

an AGC circuit which controls a gain of a modulating signal based on the signal outputted from the PLL circuit and outputs a control signal; and

a voltage controlled oscillation circuit which controls an oscillation frequency of a signal outputted from said PLL circuit based on said control signal, wherein said voltage controlled oscillation circuit includes;

a first voltage controlled reactance unit which inputs said signal output outputted from said PLL circuit; and

a second voltage controlled reactance unit which inputs said control signal; and

a high-frequency oscillation circuit connected in parallel with said first and second voltage controlled reactance units, which outputs said input signal.

Claim 2 (currently amended): The modulator as claimed in Claim 1, wherein the first voltage controlled reactance unit includes a first varactor diode and a second varactor diode, wherein the cathodes of the first varactor diode and second varactor diode are connected to each other, and the signal outputted from the PLL circuit is inputted where the cathodes are connected to each other.

Claim 3 (currently amended): The modulator as claimed in Claim 2, wherein the second voltage controlled reactance unit includes a third varactor diode and a fourth varactor diode, wherein the cathodes of the third varactor diode and fourth varactor diode are connected to each other, and the control signal is inputted where the cathodes are connected to each other.

Claim 4 (currently amended): The modulator as claimed in ~~Claim 2~~ Claim 1, wherein the PLL circuit ~~includes~~ comprises:

an oscillator that generates the reference signal[[,]];

a frequency divider that divides the frequency of the input signal ~~to output a frequency divided signal, and;~~

a comparator ~~that~~ which compares the reference signal and the frequency divided input signal to detect a phase difference ~~between both.~~

Claims 5-6 (canceled)

Claim 7 (currently amended): The modulator as claimed in Claim 1, wherein the first voltage controlled reactance unit includes a first varactor diode and a first capacitor, wherein the cathode of the first varactor diode is connected to one end of the first capacitor, and the signal outputted from the PLL circuit is inputted where the cathode and the one end are connected to each other.

Claim 8 (currently amended): The modulator as claimed in Claim ~~2~~ 7, wherein the second voltage controlled reactance unit includes a second varactor diode and a second capacitor, wherein the cathode of the second varactor diode is connected to

one end of the second capacitor, and the control signal is inputted where the cathode and the one end are connected to each other.

Claims 9-11 (canceled)

Claim 12 (original): A modulator comprising:

a PLL circuit that detects a phase difference between an input signal and a reference signal,

a selection circuit that outputs control signals on the basis of a signal outputted from the PLL circuit, and

a voltage controlled oscillation circuit that controls an oscillation frequency of the signal outputted from the PLL circuit on the basis of the control signal,

wherein the voltage controlled oscillation circuit includes:

a first voltage controlled reactance unit that inputs the signal outputted from the PLL circuit,

second and third voltage controlled reactance units that input the control signals, and

a high-frequency oscillation circuit connected in parallel with the first, second, and third voltage controlled reactance units, which outputs the input signal.

Claim 13 (currently amended): The modulator as claimed in Claim 12, wherein:

the first voltage controlled reactance unit includes a first varactor diode and a second varactor diode, in which the cathodes of the first varactor diode and second varactor diode are connected to each other, and the signal outputted from the PLL circuit is inputted where the cathodes are connected to each other;

the second voltage controlled reactance unit includes a third varactor diode and a fourth varactor diode, in which the cathodes of the third varactor diode and fourth varactor diode are connected to each other, and the control signal is inputted where the cathodes are connected to each other; and

the third voltage controlled reactance unit includes a fifth varactor diode and a sixth varactor diode, in which the cathodes of the fifth varactor diode and sixth varactor diode are connected to each other, and the control signal is inputted where the cathodes are connected to each other.

Claim 14 (original): The modulator as claimed in Claim 13, wherein the PLL circuit includes an oscillator that generates the reference signal, a frequency divider that divides the frequency of the input signal to output a frequency divided signal, and a comparator that compares the reference signal and the frequency divided signal to detect a phase difference between both.

Claim 15 (original): The modulator as claimed in Claim 13, wherein the selection circuit outputs the control signal to the second voltage controlled reactance unit, when a voltage level of the signal outputted from the PLL circuit is higher than a threshold level, and outputs the control signal to the second and third voltage controlled reactance units, when the voltage level of the signal outputted from the PLL circuit is lower than the threshold level.

Claim 16 (original): A modulator comprising:

a PLL circuit that compares phases of a reference signal and a frequency divided signal in which a frequency of an input signal is divided, and outputs a phase difference signal,

a selection circuit that outputs control signals on the basis of the frequency divided signal, and

a voltage controlled oscillation circuit that controls an oscillation frequency of the phase difference signal on the basis of the control signal,

wherein the voltage controlled oscillation circuit includes:

a first voltage controlled reactance unit that inputs the phase difference signal,

second and third voltage controlled reactance units that input the control signals, and

a high-frequency oscillation circuit connected in parallel with the first, second, and third voltage controlled reactance units, which outputs the input signal.

Claim 17 (original): The modulator as claimed in Claim 16 wherein:

the first voltage controlled reactance unit includes a first varactor diode and a second varactor diode, in which the cathodes of the first varactor diode and second varactor diode are connected to each other, and the phase difference signal is inputted where the cathodes are connected to each other;

the second voltage controlled reactance unit includes a third varactor diode and a fourth varactor diode, in which the cathodes of the third varactor diode and fourth varactor diode are connected to each other, and the control signal is inputted where the cathodes are connected to each other; and

the third voltage controlled reactance unit includes a fifth varactor diode and a sixth varactor diode, in which the cathodes of the fifth varactor diode and sixth varactor diode are connected to each other, and the control signal is inputted where the cathodes are connected to each other.

Claim 18 (original): The modulator as claimed in Claim 17, wherein the PLL circuit includes an oscillator that generates the reference signal, a frequency divider that divides the frequency of the input signal to output the frequency divided signal, and a comparator that compares the reference signal and the frequency divided signal to detect a phase difference between both.

Claim 19 (original): The modulator as claimed in Claim 17, wherein the selection circuit outputs the control signal to the second voltage controlled reactance unit, when a voltage level of the phase difference signal is higher than a threshold level, and outputs the control signal to the second and third voltage controlled reactance units, when the voltage level of the phase difference signal is lower than the threshold level.

Claim 20 (new): A modulator comprising:

- a PLL circuit which detects a phase difference between an input signal of which a frequency is divided and a reference signal;

- an AGC circuit which controls a gain of a modulating signal based on the input signal of which a frequency is divided, and which outputs a control signal; and

- a voltage controlled oscillation circuit which controls an oscillation frequency of a signal outputted from said PLL circuit based on said control signal, wherein said voltage controlled oscillation circuit includes;

- a first voltage controlled reactance unit which inputs said signal outputted from said PLL circuit;

- a second voltage controlled reactance unit which inputs said control signal; and

- a high-frequency oscillation circuit connected in parallel with said first and second voltage controlled reactance units, which outputs said input.

Claim 21 (new): The modulator according to claim 20, wherein the first voltage controlled reactance unit includes a first varactor diode and a second varactor diode, wherein the cathodes of the first and second varactor diodes are connected to each other, and wherein the signal outputted from the PLL circuit is inputted where the cathodes are connected to each other.

Claim 22 (new): The modulator according to claim 21, wherein the second voltage controlled reactance unit includes a third varactor diode and a fourth varactor diode, wherein the cathodes of the third varactor diode and fourth varactor diode are connected to each other, and wherein the control signal is inputted where the cathodes are connected to each other.

Claim 23 (new): The modulator according to claim 20, wherein the PLL circuit comprises:

- an oscillator which generates the reference signal;
- a frequency divider which divides a frequency of the input signal; and
- a comparator which compares the reference signal and the divided input signal to detect the phase difference.

Claim 24 (new): The modulator according to claim 20, wherein the first voltage controlled reactance unit includes a first varactor diode and a first capacitor, wherein a cathode of the first varactor diode is connected to one end of the first capacitor, and wherein the signal outputted from the PLL circuit is inputted where the cathode and the one end are connected to each other.

Claim 25 (new): The modulator according to claim 24, wherein the second voltage controlled reactance unit includes a second varactor diode and a second capacitor, wherein a cathode of the second varactor diode is connected to one end of the second capacitor, and wherein the control signal is inputted where the cathode and the one end are connected to each other.